

# A Temperature-insensitive Simple Current-mode Multiplier/Divider Employing Only Multiple-output CDTA

P. Silapan<sup>1</sup>, and C. Chanapormma<sup>2</sup>

<sup>1,2</sup>Uttaradit Rajabhat University/Department of Electrical Computer and Industrial, Faculty of Industrial Technology, Uttaradit, THAILAND

Email: phamorn@mail.uvu.ac.th<sup>1</sup> chaiyanc@uvu.ac.th<sup>2</sup>

**Abstract**— This article presents a new current-mode multiplier/divider based on MO-CDTA (Multiple output current conveyor transconductance amplifier). The circuit description is very simple, its construction consists of only one MO-CDTA. Without external passive elements, the proposed circuit is then suitable for IC architecture. The PSpice simulation and experimental results are depicted, and agree well with the theoretical anticipation. From simulation results, the maximum power consumption is approximately 2.14mW at  $\pm 2V$  power supply voltages.

**Index Terms**— multiplier/divider, current-mode, MO-CDTA

## I. INTRODUCTION

A multiplier and divider has been found for wide usefulness in analog instrumentation and measurement systems, such amplitude modulator, and de modulator [1-3]. From literature review, it found that several implementations of square-rooting circuits using different high-performance active building blocks such as, OTAs [4], current conveyors (CCIs) [5], current controlled current conveyors [6], current differencing buffered amplifiers (CDBAs) [7], have been reported. Unfortunately, these reported circuits suffer from one or more of following weaknesses:

- Excessive use of the active/passive elements, especially external resistors [4-6].
- Depending on ambient temperature of output [4,7].

Presently, a current-mode technique [8] has being been more popular than voltage-mode one. This is due to requirements in low-voltage environment such as in portable and battery-powered equipments. Since a low-voltage operating circuit becomes necessary, the current-mode technique is ideally suited for this purpose. Presently, there is a growing interest in synthesizing the current-mode circuits because of more their potential advantages such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and lower power consumption [8-9]. The current differencing transconductance amplifier (CDTA) [10] seems to be a versatile component in the realization of a class of analog signal processing circuits. It is really current-mode element whose input and output signals are currents. In addition, it can be adjusted the output current gain. The purpose of this paper is to introduce a novel current-mode multiplier/divider based on use of MO-CDTA. The features of the proposed multiplier/divider are that; the proposed multiplier/divider can multiply and divide two current signals throughout four-quadrant and two-quadrant, respectively, without changing

the circuit topology: the circuit is ideally insensitive to temperature variations: the output current can be controlled via input bias currents.; magnitude of output signal is ideally temperature-insensitive; the proposed circuit consists of 4 CC-CDBAs and without any passive element, which is appropriate to fabricate in integrated circuit architecture. The PSpice simulation and experimental results are also shown, which are in correspondence with the theoretical analysis.

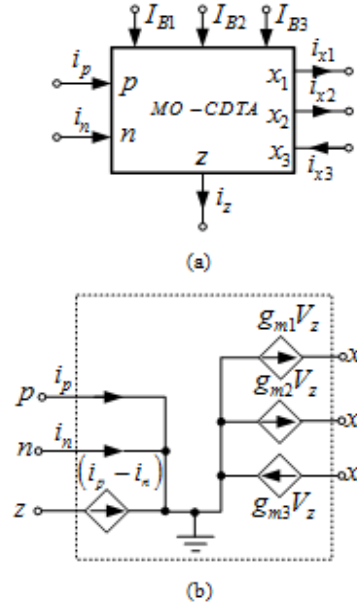


Figure 1. The MO-CDTA (a) symbol (b) equivalent circuit

## II. PRINCIPLE OF OPERATION

### A. Basic Concept of MO-CDTA

Since the proposed circuit based on MO-CDTA, a brief review of the MO-CDTA is given in this section. The voltage and current relationships of MO-CDTA are shown in (1)

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_{x1} \\ I_{x2} \\ I_{x3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & g_{m1} & 0 & 0 & 0 \\ 0 & 0 & g_{m2} & 0 & 0 & 0 \\ 0 & 0 & -g_{m3} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_{x1} \\ V_{x2} \\ V_{x3} \end{bmatrix} \quad (1)$$

where

$$g_{m1} = \frac{I_{B1}}{2V_T}, g_{m2} = \frac{I_{B2}}{2V_T}, g_{m3} = \frac{I_{B3}}{2V_T}. \quad (2)$$

$g_{m1}$ ,  $g_{m2}$ , and  $g_{m3}$  are the transconductances of the MO-CDTA.  $V_T$  is the thermal voltage. The symbol and the equivalent circuit of the MO-CDTA are illustrated in Figs. 1(a) and (b), respectively.

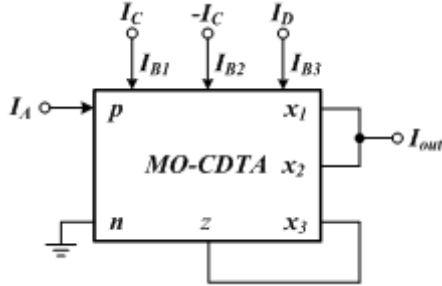


Figure. 2. Circuit diagram of proposed current-mode multiplier/divider

### B. The proposed Current-mode Multiplier/Divider

The proposed current-mode multiplier/divider using the MO-CDTA is displayed in Fig. 2. By routine analysis circuit in Fig. 2 and using the properties of MO-CDTA in Section II.A, the output current at z terminal of MO-CDTA is obtained by

$$I_z = I_A = -I_{x3}. \quad (3)$$

Then, the output voltage at z terminal ( $V_z$ ) of MO-CDTA can be found to be

$$V_z = -\frac{I_{x3}}{g_{m3}} = \frac{2V_T I_A}{I_{B3}}. \quad (4)$$

From Fig. 2, it is found that  $I_{B1} = I_C$ ,  $I_{B2} = -I_C$  and  $I_{B3} = I_D$

Thus, the  $I_{x1}$  and  $I_{x2}$  can be obtained by

$$I_{x1} = \begin{cases} g_{m1} V_z & \text{if } I_C > 0 \\ 0 & \text{if } I_C < 0 \end{cases} = \begin{cases} \frac{I_A I_C}{I_D} & \text{if } I_C > 0 \\ 0 & \text{if } I_C < 0 \end{cases}, \quad (5)$$

and

$$I_{x2} = \begin{cases} 0 & \text{if } I_C > 0 \\ g_{m2} V_z & \text{if } I_C < 0 \end{cases} = \begin{cases} 0 & \text{if } I_C > 0 \\ -\frac{I_A I_C}{I_D} & \text{if } I_C < 0 \end{cases}. \quad (6)$$

From (5)-(6), the output current ( $I_{out}$ ) of the multiplier/divider is displayed as

$$I_{out} = I_{x1} + I_{x2} = \frac{I_A |I_C|}{I_D}. \quad (7)$$

From (7), it is clearly seen that, if  $I_A$  and  $I_C$  are assigned to be input currents, the proposed circuit serves as a current-

mode 4 quadrant multiplier because  $I_A$  and  $I_C$  can be either a positive or a negative value. If either  $I_A$  or  $I_C$  and  $I_D$  are the input currents, the proposed circuit can work as a current-mode divider. Due to being a positive value of  $I_D$ , the proposed circuit can be 2 quadrant divider. Furthermore, in ideal case, it is temperature-insensitive owing to no term of  $V_T$ .

### C. Non Ideal Case

For non-ideal case, the MO-CDTA can be characterized by.

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_{x1} \\ I_{x2} \\ I_{x3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 & 0 & 0 \\ 0 & 0 & \gamma g_{m1} & 0 & 0 & 0 \\ 0 & 0 & \gamma g_{m2} & 0 & 0 & 0 \\ 0 & 0 & -\gamma g_{m3} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_{x1} \\ V_{x2} \\ V_{x3} \end{bmatrix} \quad (8)$$

where  $\alpha_p$ ,  $\alpha_n$  and  $\gamma$  are transferred values, these values can be deviated from one. In the case of non-ideal and reanalyzing the proposed multiplier/divider in Fig. 2, it yields the output current as

$$I_{out} = \frac{\alpha_p I_A |I_C|}{I_D}. \quad (9)$$

From (9), it is found that the proposed multiplier/divider still functions as a multiplier/divider. These deviated values effect on only output magnitude. Practically, the  $\alpha_p$ ,  $\alpha_n$  and  $\gamma$  originate from intrinsic resistances and stray capacitances in the MO-CDTA. These errors affect the sensitivity to temperature and high frequency response of the proposed circuit. Consequently, the MO-CDTA should be carefully designed to achieve these errors as low as possible.

## II. SIMULATION AND EXPERIMENTAL RESULTS

To prove the performances of the proposed multiplier/divider circuit, the PSpice simulation program was used for the first examination. The PNP and NPN transistors employed in the proposed circuit were simulated by respectively using the parameter of the NR200N and PR200N bipolar transistors of ALA400 transistor array from AT&T [12]. Fig. 3 depicts schematic description of the MO-CDTA used in the simulations. The MO-CDTA was biased with  $\pm 2V$ , where  $I_A$  was set to  $100\mu A$ . The DC transfer characteristic of the proposed circuit is shown in Fig. 4.

The results in transient responses of the multiplier/divider circuit for sinusoidal and triangular inputs are displayed in Fig. 5.

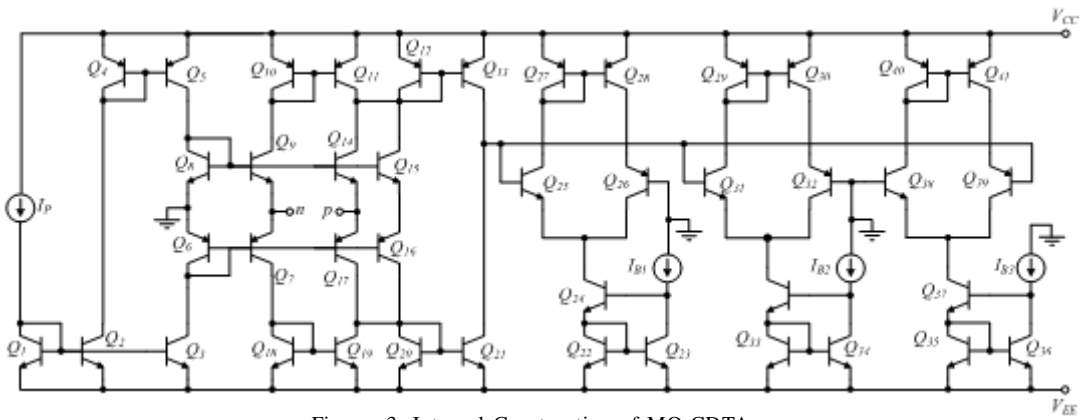


Figure. 3. Internal Construction of MO-CDTA

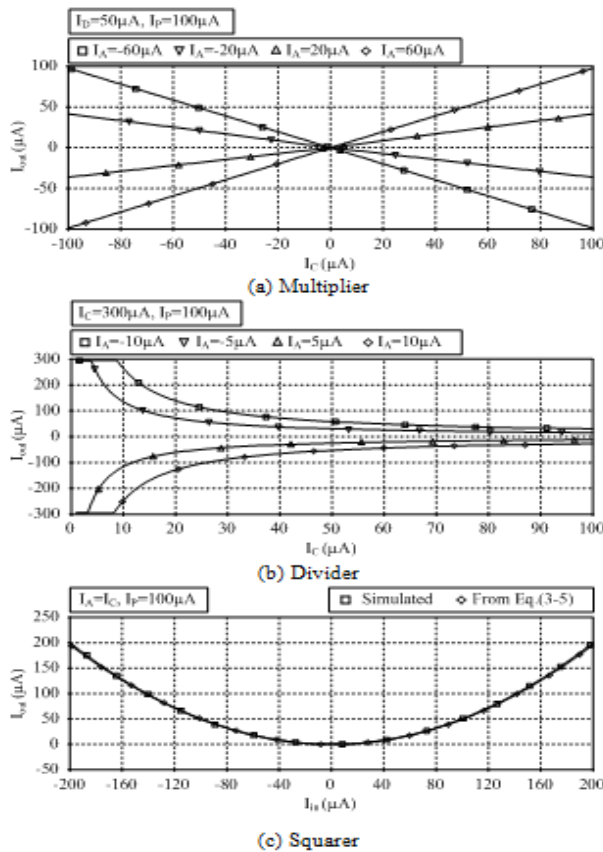


Figure4. DC transfer characteristic of the proposed multiplier/divider

Fig. 7 shows the output signal of the proposed circuit relative to temperature variations from  $27^{\circ}\text{C}$ ,  $50^{\circ}\text{C}$  and  $100^{\circ}\text{C}$ . It is clearly seen that the output current is slightly dependent on the temperature variations due to the intrinsic resistances and stray capacitances in the MO-CDTA, as depicted in Section II.C.

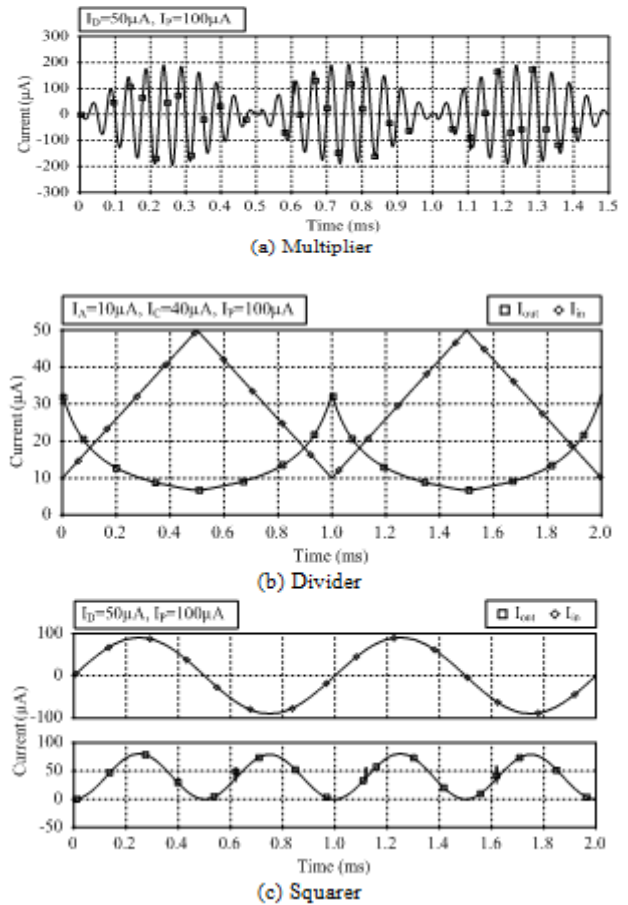


Figure 5. Transient responses of the proposed multiplier/divider

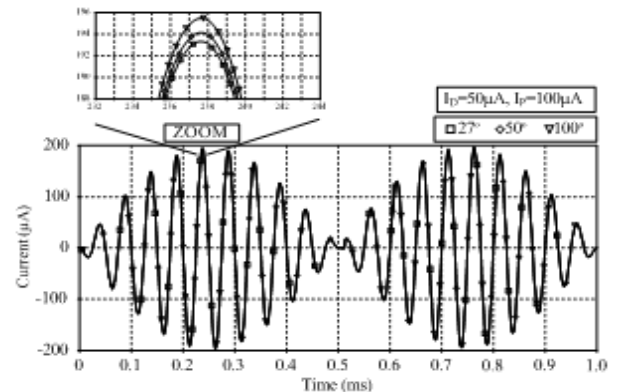


Figure 6. The output current deviations for different temperature values

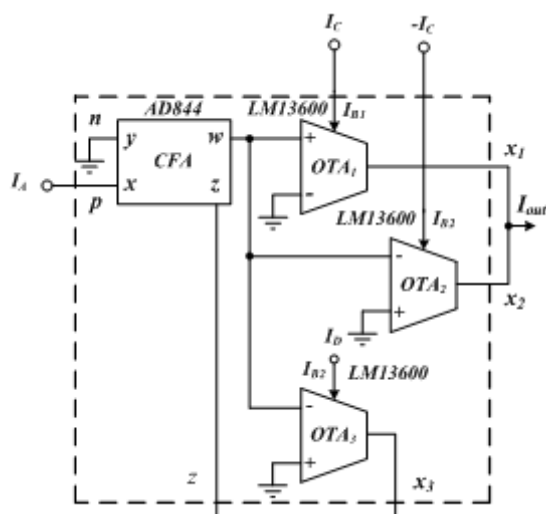


Figure 7. Practical implementation of the proposed circuit

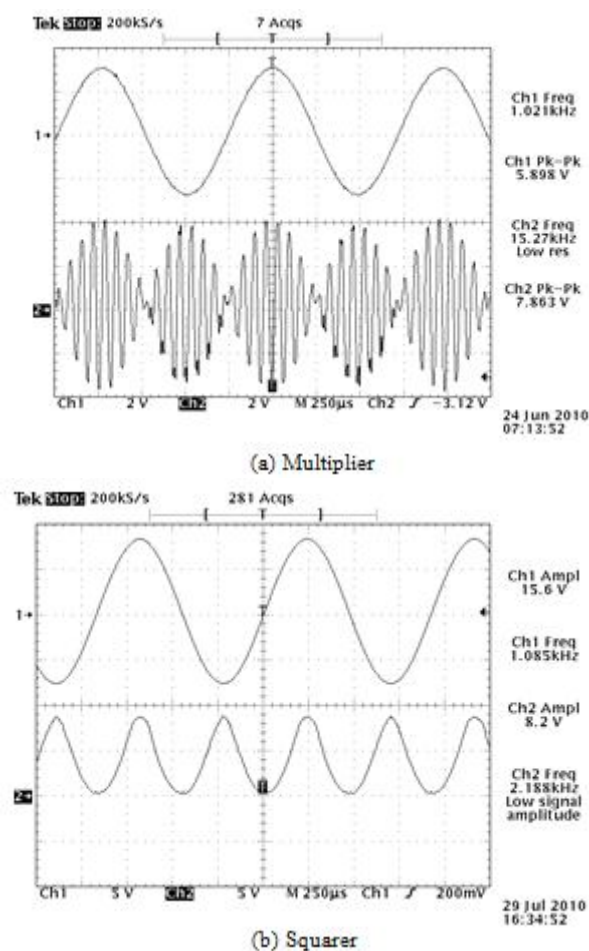


Figure 8. The experimental results of the proposed circuit

To validate that the multiplier/divider can operate practically, it was constructed using commercial ICs, as shown in Fig. 7. Figs. 8(a) and (b) show the experimental results of the proposed circuit.

#### CONCLUSIONS

The current-mode multiplier/divider based on the MO-CDTAs has been presented. The features of the proposed

circuit are that: output gain can be adjusted via input bias current; magnitude of output signal is theoretically temperature-insensitive; the proposed multiplier/divider consists of only one MO-CDTA without any passive element, which is appropriate to fabricate in integrated circuit architecture. The performances of the proposed circuit have been also investigated and discussed through PSpice simulation and experimental results. They show that the proposed circuit can function as a current-mode multiplier/divider for input current range variation from  $-200\mu\text{A}$  to  $200\mu\text{A}$ . From simulation results, the maximum power consumption is  $2.14\text{mW}$  at  $\pm 2\text{V}$  supply voltages. The maximum error of the amplitude of output current signal due to variations of the temperature from  $0-100^\circ\text{C}$  is approximately  $0.16\%$ .

#### ACKNOWLEDGMENT

This work was supported in part by a grant from the Research and Development Institute, Uttaradit Rajabhat University (URU).

#### REFERENCES

- [1] D. M. W. Leenaerts, G. H. M. Joordens, and J. A. Hegt, "A  $3.3\text{V}$   $625\text{kHz}$  switched-current multiplier," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1340-1343, Sep. 1996.
- [2] M. A. Abou El-Atta, M. A. Abou El-Ela, and M.K. El Said, "Four-quadrant current multiplier and its application as a phase-detector," *Proceedings of the Nineteenth National Radio Science Conference (NRSC 2002)*, pp. 502-508, Mar. 2002.
- [3] H. Wasaki, Y. Horio, and S. Nakamura, "Current multiplier/divider circuit," *Electronics Letters*, vol. 27, no. 6, pp. 504-506, Mar. 1991.
- [4] S. Maheshwari, and I. A. Khan, "Current-controlled current differencing buffered amplifier: implementation and applications," *Active and Passive Electronic Components*, vol. 4, pp. 219-227, 2004.
- [5] C. Premont, S. Cattet, R. Grisel, N. Abouchi, J. P. Chante, and D. Renault, "A CMOS multiplier/divider based on current conveyors," *Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 69-71, 1998.
- [6] K. Kaewdang, C. Fogsamut and W. Surakamponorn, "A Wide-Band. Current-Mode OTA-Based Analog Multiplier-Divider," *ISCAS'03*, vol. 1, pp. I-349 - I-352, 2003.
- [7] A. Ü. Keskin, "A Four Quadrant Analog Multiplier Employing Single CDBA," *Analog Integrated Circuits and Signal Processing*, vol. 40 n.1, pp.99-101, July 2004.
- [8] C. Toumazou, F. J. Lidgey and D. G. Haigh. *Analogue IC design: the current-mode approach*, London: Peter Peregrinus, 1990.
- [9] H. Schmid, "Why the terms 'current mode' and 'voltage mode' neither divide nor qualify circuits," *IEEE ISCAS*, pp. II-29-II-32, 2002.
- [10] D. Birolek, "CDTA – Building block for current-mode analog signal processing," *Proceedings of the European conference on circuit theory and design 2003 - ECCTD'03*, 2003, pp. 397-400, 2003.
- [11] D.R. Frey "Log-domain filtering: an approach to current-mode filtering". *IEE Proc. Circuit Devices Syst.*, vol. 140, pp. 406-416, 1993.